Docket No.: 060188-0550 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Nobuaki TARUMI, et al.	:	Confirmation Number: 4739
Application No.: 10/613,048 Patent No.: 6,951,809 B2	:	Group Art Unit: 2829
Filed: July 07, 2003 Issued: October 4, 2005	:	Examiner: Asok K. Sarkar

For: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR 1.322

Mail Stop CERTIFICATE OF CORRECTION
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In reviewing the above-identified patent, a printing error was discovered therein requiring correction in order to conform the Official Record in the application.

The error noted is set forth on the attached copy of form PTO-1050 Rev. 2-93 in the manner required by the Commissioner's Notice.

Specifically, in printed claim 7 (originally claim 14), Column 9, lines 7 - 8, change "RE power" to - - **RF** power - -. A copy of Applicants' Amendment filed September 29, 2004 showing the correct version of the text is attached for your information and convenience.

The change requested herein occurred as a result of printing the Letters Patent and the Certificate should be issued without expense under Rule 322 of the Rules of Practice. Accordingly, Applicants request issuance of the Certificate of Correction.

Please charge any shortage in fees due in connection with the filing of this paper to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Ramyar M. Farid
Registration No. 46,692

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 RMF:bd
Facsimile: 202.756.8087
Date: August 16, 2006

Please recognize our Customer No. 20277 as our correspondence address.

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

APPLICATION NO.: 10/613,048

PATENT NO. : 6,951,809 B2

DATED : October 04, 2005

INVENTOR(S): Nobuaki TARUMI, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

IN THE CLAIMS:

Column 9, line 7 – 8, change "RE power" to - - **RF** power - -.

Applicant: Nobuaki TARUMI, et al. Docket No. 60188-550

Title: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE Serial/Reg./Patent No. 10/613,048

Date Sent: 9/29/2004 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ First Class Mail ☐ Express Mail No. _____

☐ Transmittal Letter

New Patent App ☐ Utility ☐ Design ☐ Cont. ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

☐ Other: _____

_____ pages of Specification

_____ pages of Claims

_____ pages of Abstract

_____ pages of Formal/Informal Drawings

☐ Small Entity ☐ Large Entity

☐ Declaration/Power of Attorney

☐ Recordation of Assignment/Security Agreement

☐ Information Disclosure Statement

_____ Form PTO 1449

_____ copies of cited references

☐ Preliminary Amendment

☐ Response to Missing Parts Notice

☐ Resp. to Notice to Correct App. Papers

☐ Certified Copy of Priority Doc.

☐ Claim for Convention Priority

☒ Response/Amendment to Office Action of June 30, 2004

☐ Request for _____ month Extension of Time

☐ Letter submitting _____ pages of drawings

☐ Req. for Approval of Drawing Amendments

☐ Req. for Oral Hearing

☐ Not. of Appeal ☐ Appeal Brief ☐ Reply Brief

☐ Rule 312 Amendment/Letter

☐ Req. for Acknowledgement of Cited Art

☐ Issue Fee

☐ Publication Fee

☐ Req. for Certificate of Correction

☐ Maintenance Fee for _____ years after grant

☐ Fee Address Indication Form

☐ Terminal Disclaimer

☐ Petition to Commissioner

☐ Status Inquiry

☐ Other _____

Check for $		☐ Charge Deposit Acct. 500417$	0	Atty Init.	RMF	Tkpr. #	5328	Secy. or PL:	RHarris

CMS Descrip.: _____

THE PATENT AND TRADEMARK OFFICE DATE STAMPED HEREON IS ACKNOWLEDGEMENT THAT THE ITEMS, CHECKED ABOVE, WERE RECEIVED BY THE PTO ON THE DATE STAMPED.

Docket No.: 60188-550

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Nobuaki TARUMI, et al.	:	Confirmation Number: 4739
Application No.: 10/613,048	:	Group Art Unit: 2829
Filed: July 07, 2003	:	Examiner: Asok K. Sarkar

For: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is an Amendment in the above-identified application.

☒ No additional fee is required.
☐ Applicant is entitled to small entity status under 37 CFR 1.27
☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	14	20	0	$18.00 =	$0.00
Independent Claims	2	3	0	$86.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
		Total of Above Calculations			$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP

Ramyar M. Farid
Registration No. 46,692

600 13th Street, N.W.
Washington, DC 20005-3096
202.756.8000 RMF:rrh
Facsimile: 202.756.8087
Date: September 29, 2004

Docket No.: 60188-550 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Application No.: 10/613,048	:	Group Art Unit: 2829
Filed: July 07, 2003	:	Examiner: Asok K. Sarkar

For: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated June 30, 2004, having a three-month shortened statutory period for response set to expire on September 30, 2004, reconsideration of the above-identified application is respectfully requested in view of the following amendment and remarks.

AMENDMENT TO THE CLAIMS

1. (Currently Amended) A method for manufacturing a semiconductor device comprising:

a first step of forming an insulating film including a contact hole on a substrate;

a second step of forming a conductive underlying layer on the insulating film inclusive of the sidewall surface and the bottom surface of the contact hole;

a third step of subjecting the underlying layer to sputter-etching so that a part of the underlying layer deposited on the bottom surface of the contact hole is at least partially deposited on the lower part of the sidewall surface of the contact hole; and

a fourth step of forming a metal layer on the underlying layer by plating,

wherein in the third step, a film thickness of the underlying layer deposited on the lower part of the sidewall surface of the contact hole increases while a part of the underlying layer remains on the bottom surface of the contact hole.

2. (Original) The method for manufacturing the semiconductor device of Claim 1 wherein

the underlying layer is a plating seed layer made of metal, and

the plating seed layer and the metal layer contain copper as a main ingredient.

3. (Original) The method for manufacturing a semiconductor device of Claim 1 wherein

the underlying layer is a barrier layer for preventing atoms constituting the metal layer from diffusing into the insulating film, and

the method further comprises, between the third step and the fourth step, a fifth step of forming a plating seed layer made of metal on the barrier layer inclusive of the sidewall surface and the bottom surface of the contact hole.

4. (Currently Amended) The method for manufacturing a semiconductor device of Claim 3, said method further comprising, between the fifth step and the fourth step, a sixth step of subjecting the plating seed layer to sputter-etching so that a part of the plating seed layer deposited on the bottom surface of the contact hole is at least partially deposited on the lower part of the sidewall surface of the contact hole,

wherein in the sixth step, a film thickness of the plating seed layer deposited on the lower part of the sidewall surface of the contact hole increases while a part of the plating seed layer remains on the bottom surface of the contact hole.

5. (Original) The method for manufacturing a semiconductor device of Claim 3 wherein the plating seed layer and the metal layer contain copper as a main ingredient.

6. (Original) The method for manufacturing a semiconductor device of Claim 3 wherein in the third step, a portion of the barrier layer deposited on the bottom surface of the contact hole is removed.

7. (Original) The method for manufacturing a semiconductor device of Claim 3 wherein the barrier layer is made of high melting point metal or nitride of the high melting point metal.

8. (Original) The method for manufacturing a semiconductor device of Claim 3 wherein the barrier layer comprises a lower barrier layer made of nitride of high melting point metal and an upper barrier layer made of high melting point metal, and

the second and third steps are performed for each of the lower barrier layer and the upper barrier layer.

9. (New) The method for manufacturing a semiconductor device of Claim 1, wherein in the third step, an overhang portion of the underlying layer at the upper end of an opening of the contact hole decreases while the film thickness of the underlying layer deposited on the lower part of the sidewall surface of the contact hole increases.

10. (New) The method for manufacturing a semiconductor device of Claim 1, wherein in the third step, the contact hole is uniformly covered with the underlying layer while the film thickness of the underlying layer deposited on the lower part of the sidewall surface of the contact hole increases.

11. (New) The method for manufacturing a semiconductor device of Claim 1, wherein in the second step, the underlying layer is deposited by a sputtering method in which DC source power is applied to a target, and

in the third step, the DC source power is reduced, RF power is applied to the substrate, and a sputter-etching process employing argon gas is performed to the underlying layer.

12. (New) The method for manufacturing a semiconductor device of Claim 4, wherein in the sixth step, an overhang portion of the plating seed layer at the upper end of an opening of the contact hole decreases while the film thickness of the plating seed layer deposited on the lower part of the sidewall surface of the contact hole increases.

13. (New) The method for manufacturing a semiconductor device of Claim 4, wherein in the sixth step, the contact hole is uniformly covered with the plating seed layer while the film thickness of the plating seed layer deposited on the lower part of the sidewall surface of the contact hole increases.

14. (New) The method for manufacturing a semiconductor device of Claim 4, wherein in the fifth step, the plating seed layer is deposited by a sputtering method in which DC source power is applied to a target, and

in the sixth step, the DC source power is reduced, RF power is applied to the substrate, and a sputter-etching process employing argon gas is performed to the plating seed layer.

REMARKS

Claims 1, 3 and 5-8 stand rejected under 35 U.S.C. § 102 as being anticipated by Chen et al. '091 ("Chen"), and claims 2, 4 stand rejected under 35 U.S.C. § 103 as being unpatentable over Chen in view of Gopalraja et al. '177 ("Gopalraja"). Claim 1 is the sole independent claim. These rejections are respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "a third step of subjecting the underlying layer to sputter-etching so that a part of the underlying layer deposited on the bottom surface of the contact hole is at least partially deposited on the lower part of the sidewall surface of the contact hole ... wherein in the third step, a film thickness of the underlying layer deposited on the lower part of the sidewall surface of the contact hole increases while a part of the underlying layer remains on the bottom surface of the contact hole." Support for this feature can be found, for example, on page 4, lines 10-16 of Applicants' specification and Figures 2A,B of Applicants' drawings. In contrast, Chen expressly discloses removal of the bottom portion 32 of the barrier layer 30 (*see* col. 4, lines 62-64 and Figure 3).

Gopalraja, on the other hand, discloses a sputter ***deposition*** process (by depositing copper ions with high-energy sputtering and by resputtering the copper) rather than a sputter-***etch*** process as part of the alleged third step. Indeed, Gopalraja teaches away from using a sputter-etch process (*see, e.g.,* col. 6, lines 35+ of Gopalraja, which expressly teaches away from using a sputter-etch step).

According to one aspect of the present invention, because the underlying layer (or the plating seed layer) can be continuously deposited on the lower part of the sidewall surface of the contact hole, the coverage of the underlying (or the plating seed layer) can be improved so as to enable the prevention of step discontinuity described in Applicants' specification with respect to the

admitted prior art shown in Figures 7-10 of Applicants' drawings. Only Applicants have recognized and considered such a problem, and conceived of a means by which to enable prevention thereof.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Chen does not anticipate claim 1, nor any claim dependent thereon.

The Examiner is further directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 1 because the cited prior art, alone or in combination, fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

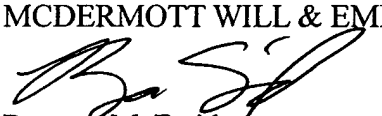
CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



Ramyar M. Farid
Registration No. 46,692

600 13th Street, N.W.
Washington, DC 20005-3096
202.756.8000 RMF:rrh
Facsimile: 202.756.8087
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